Thesis title:

Reliable and Trustworthy Neuromorphic Computing with Spiking Neural Networks

Institution:

Sorbonne Université
French National Centre for Scientific Research (CNRS)
Computer Science Laboratory of Sorbonne University's Faculty of Science and Engineering (LIP6)
Sorbonne Center for Artificial Intelligence (SCAI)

Location:

Paris, France

When:

Starting September or October 2023

Funding:

3 year PhD grant, ~2000€ monthly gross salary, social security benefits included.

Advisors:

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Context:

The biological brain is the most brilliant computing machine. It is very “green” consuming only 12W with a computational power efficiency that is higher than computers by orders of magnitude. While computers can do computations much faster, the biological brain has augmented capabilities such as learning, producing new ideas, interpreting the outside world, and making up for damage. This has motivated scientists to build neuromorphic processors that emulate brain-like functionality.

Neuromorphic computing is an emerging computing paradigm aiming at solving various problems, such as visual sensing and perception, control-loops for robotics, brain-computer interfacing, audio processing, etc., with comparative advantage to the contemporary von Neumann computing architecture as well as the classical artificial neural networks (ANNs). Neuromorphic computing has as basis a spiking neural network (SNN) which is considered to be the third generation of neural networks [1]. Input information is coded into spike trains and spikes, or events, propagate asynchronously through the layers of the network. This event-based operation as well as the sparsity of events enable a very low-power operation. Nowadays, there is intense activity in designing circuital implementations of SNNs with some large-scale hardware platforms already available for research purposes [2-4] and several chips demonstrated by academic groups [5].

Given the forecasted high-volume industrialization of neuromorphic processors in the near future and their deployment in an ever-increasing number of applications, their trustworthiness aspects need to be carefully addressed in parallel to the design task [6]. Trustworthiness is a crucial requirement for correct use of AI systems and key for their mass proliferation in our daily lives. The high-level expert group on AI set up by the European Commission recently published ethics guidelines for trustworthy use of AI systems [7]. The second requirement concerns the technical robustness and safety. Even if the AI algorithms are proven to provide accurate and explainable decisions, this is under the assumption that the AI processor onto which they are executed is error-free. While we can guarantee its correctness by design, during the lifetime many hardware-level faults could emerge, for example due to silicon aging, environmental stressing, and cosmic radiation. These faults will affect the hardware and, in turn, the AI algorithms that run on it, resulting in erroneous or misleading AI decisions. Therefore, the trustworthiness of an AI system is conditioned on the trustworthiness of the hardware itself. On the other hand, many “killer” AI applications are safety-critical or mission-critical demanding high reliability, i.e., smart healthcare, robotics, autonomous vehicles, etc.

The assumption that neuromorphic processors are inherently fault-tolerant since they are modeled after the architecture and operation principles of biological neural networks has been proven false as demonstrated by recent fault injection experiments [8-9]. The over-provisioning, massive spatial redundancy, and parallel computing help to learn around even very high hardware-level fault densities; however, a hardware-level fault occurring after training in the field of application can have detrimental effect on the inference and, thus, can seriously jeopardize the application.

This PhD will focus on exploring the architectural particularities of neuromorphic processors to achieve cost-effective, low-overhead, and holistic test and reliability solutions. This includes the resiliency analysis to hardware-level faults taking into consideration reliability requirements as early as in the design phase, comprehensive and fast post-manufacturing testing to verify functionality at time zero, detecting reliability hazards and hardware-level faults in real-time when they occur in the field of application, and taking corrective actions using fault-tolerance, self-repair, error recovery, or self-healing principles to prevent failures and ensure an uninterrupted application. The long-term impact will be the design of reliable and trustworthy neuromorphic processors, “explaining” the AI hardware to remove any uncertainties originating from the hardware when attempting to explain and interpret AI decisions, prolonging the lifespan of edge devices with embedded AI, and proliferating AI solutions in new application areas with stringent reliability standards.

Short Bibliography:

[1] K. Roy, A. Jaiswal A, and P. Panda P, “Towards spike-based machine intelligence with neuromorphic computing,” Nature, vol. 575, no. 7784, pp. 607-617, 2019.

[2] E. Painkras *et al.*, “SpiNNaker: A 1-W 18-core system-on-chip for massively-parallel neural network simulation,” IEEE J. Solid-State Circuits, vol. 48, no. 8, pp. 1943–1953, 2013.

[3] P. A. Merolla *et al.*, “A million spiking-neuron integrated circuit with a scalable communication network and interface,” Science, vol. 345, no. 6197, pp. 668–673, 2014.

[4] M. Davies *et al.*, “Loihi: A neuromorphic manycore processor with on-chip learning,” IEEE Micro, vol. 38, no. 1, pp. 82–99, 2018.

[5] A. Basu, L. Deng, C. Frenkel and X. Zhang, "Spiking Neural Network Integrated Circuits: A Review of Trends and Future Directions," in Proc. IEEE Cust. Integr. Circuits Conf. (CICC), 2022.

[6] F. Su, C. Liu, and H.-G. Stratigopoulos, “Testability and Dependability of AI Hardware: Survey, Trends, Challenges, and Perspectives,” IEEE Des. Test, vol. 40, no. 2, pp. 8-58, 2023.

[7] European Commission. (Apr. 2019). Ethics Guidelines for Trustworthy Artificial Intelligence (AI). [Online]. Available: https://digital-strategy.ec.europa.eu/en/library/ethics-guidelines-trustworthy-ai

[8] C. D. Schuman et al., “Resilience and robustness of spiking neural networks for neuromorphic systems,” in Proc. Int. Jt. Conf. Neural Netw. (IJCNN), 2020.

[9] T. Spyrou, S. A. El-Sayed, E. Afacan, L. A. Camuñas-Mesa, B. Linares-Barranco, and H.-G. Stratigopoulos, “Neuron fault tolerance in spiking neural networks,” in Proc. Design Autom. Test Europe Conf. (DATE), 2021, pp. 743–748

[10] S. A. El-Sayed, T. Spyrou, L. A. Camuñas-Mesa, and H.-G. Stratigopoulos, “Compact functional testing for neuromorphic computing circuits,” IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., 2022, early access

Expected skills:

We seek a highly motivated talent with a M.Sc. degree or equivalent in Electrical Engineering or Computer Engineering and with background knowledge on circuit design, machine learning, and artificial intelligence.

How to apply:

Send by e-mail a detailed CV to Haralampos-G. Stratigopoulos (e-mail: haralampos.stratigopoulos@lip6.fr).